| Offset | PCB         | DAH | DCH | CAH | ACH | AEH | ECH | CEH | D8H | A0H | 6AH | A6H | 2AH | A4H | C0H | 7CH | 6CH | C2H | 8EH | 1EH | E6H | F2H | F4H | F0H | F8H | 32H |
|--------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|         |             |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

† this bit is ignored for unsynchronous transfers (bit is treated as being set)

* This bit must be set in cascade mode

D1DSTL DMA Channel 1 Destination Address Pointer Low DMA Channel 1 Destination Address Bits 15 to 0
D1DSTH DMA Channel 1 Destination Address Pointer High
D0CON DMA Channel 0 Control Destination is
D0DSTL DMA Channel 0 Destination Address Pointer Low DMA Channel 0 Destination Address Bits 15 to 0
D1SRCH DMA Channel 1 Source Address Pointer High
D0SRCH DMA Channel 0 Source Address Pointer High

TCUCON Timer Interrupt Control Master Mode
IMASK Interrupt Mask Master Mode
TCU2CON Timer 2 Interrupt Control Slave Mode

Notes

Halt DMA
Interrupt Request Slave Mode
Interrupt Mask Slave Mode

PCS6 PACS 15:6 + 768 (300H) PACS 15:6 + 895 (37FH)
Chip Select Starting Address Ending Address

PCS Active Range

801C88XL Peripheral Control Block (PCB) Registers